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The LCD(M) Specialist

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PART NO. : PQG1203A-SYL

FOR MESSRS. : _____

CONTENTS

龐誼科技
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發行

ACCEPTED BY : _____ PROPOSED BY : _____

RECORD OF REVISION

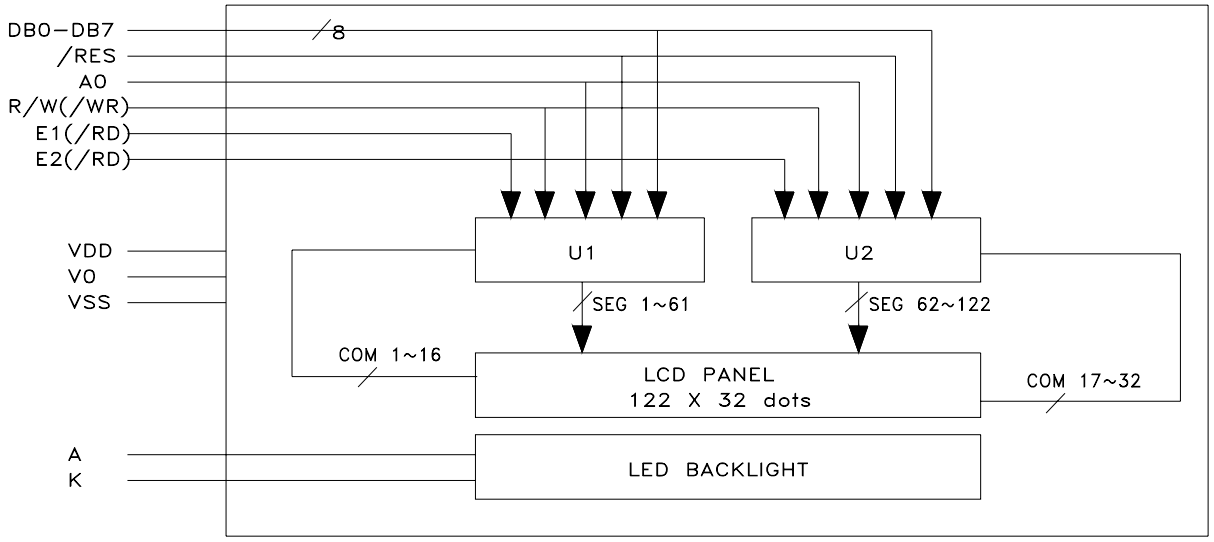
DATE	PAGE	SUMMARY
2007/01/16	P4	FIRST ISSUE

1 . SPECIFICATIONS

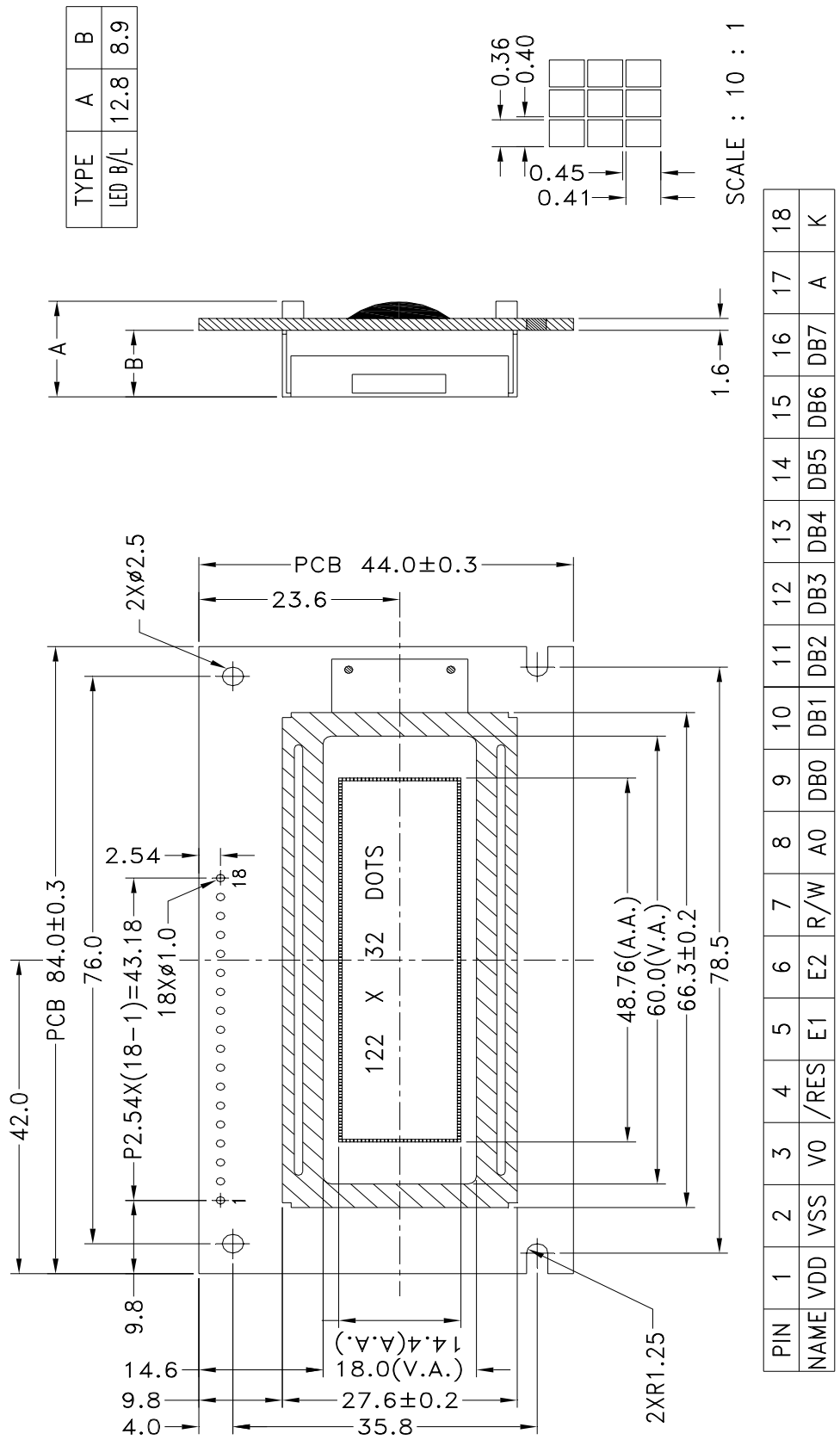
1.1 FEATURES

Item	Contents	Unit
LCD TYPE	STN/Transflective/Positive/Y-G	--
LCD duty	1/32	--
LCD bias	1/6	--
Viewing direction	6	o'clock
Operation Temperature	-10℃--+60℃	
Storage Temperature	-20℃--+70℃	
Module size(W x H x T)	84.0 X 44.0 X 12.8	mm
Viewing area(W x H)	60.0 X 18.0	mm
Number of dots	122 X 32	dots
Dots size(W x H)	0.36 X 0.41	mm
Dots pitch(W x H)	0.40 X 0.45	mm
LED backlight	Yello-green	

1.2. BLOCK DIAGRAM



1.3. MECHANICAL SPECIFICATION



SPECIFICATIONS

1. DISPLAY TYPE: STN/TRANSFLECTIVE/POSITIVE/Y-G
2. LCD DRIVING VOLTAGE: 5.0V
3. LOGIC VOLTAGE: 5.0V
4. VIEWING DIRECTION: 6 O'CLOCK
5. OPERATING TEMP: -10°C~60°C
6. STORAGE TEMP: -20°C~70°C
7. DRIVE MODE: 1/32 DUTY,1/6 BIAS
8. BACKLIGHT: YELLOW GREEN/BOTTOM BACKLIGHT/5.0V
9. CONTROL/DRIVE IC: AT1520OA
10. OTHER:
MECHANICAL TOL.±0.2 UNLESS SPECIFIED

1.4 ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VSS	0	5.5	V
Supply voltage for LCD	Vo	Vdd –V5	13.0	V
Input voltage	VI	VSS -0.3	+0.3	V
Normal operating temperature	Topr	-10	+60	℃
Normal storage temperature	Tstg	-20	+70	℃

Notes: 1. All voltages are specified relative to VDD = 5.0 V.

2. The following relation must be always hold
   VDD≧V1 ≧V2 ≧V3 ≧V4 ≧V5
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

1.5 DC ELECTRICAL CHARACTERISTIC

Ta = –10 to 60℃, VDD = 5.0V unless stated otherwise

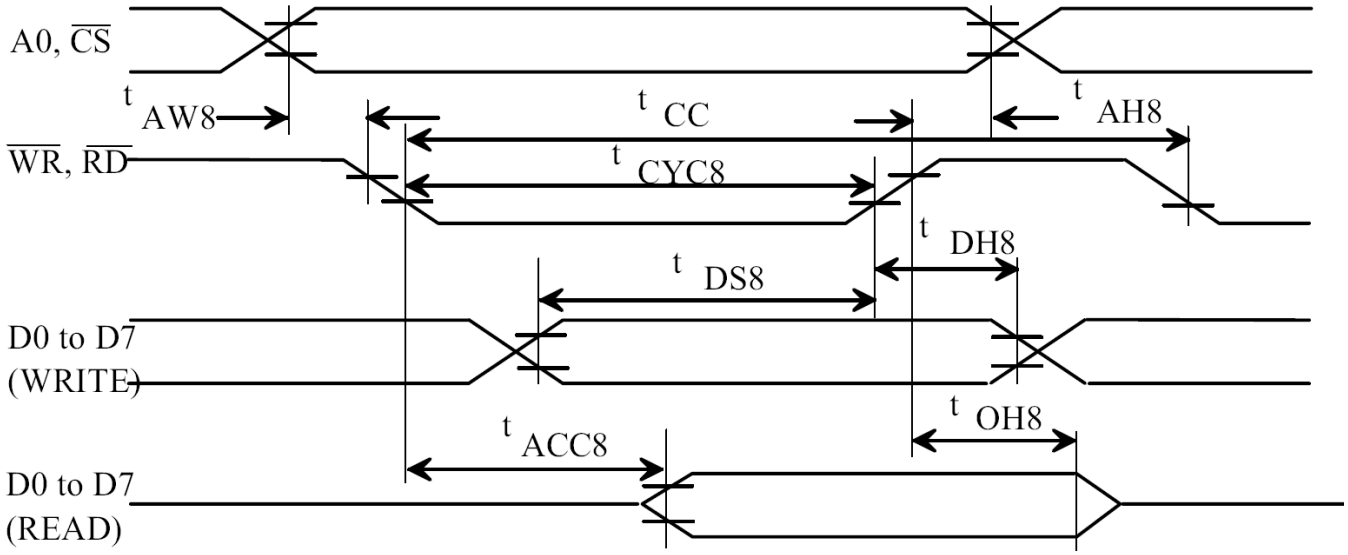
Parameter	Symbol	Condition		Rating			Unit	Applicable Pin
				min	typ	max		
High-level output voltage	VOHT	IOH=-3.0 mA		Vss+2.7	--	--	V	OSC2 See note 4 & 5.
	VOHC1	IOH=-2.0mA		Vss+2.7	--	--		
	VOHC2	IOH=-120 μ		0.2xVss	--	--		
Low-level output voltage	VOLT	IOL=3.0mA		--	--	Vss+0.4	V	OSC2 See note 4 & 5.
	VOLC1	IOL=2.0mA		--	--	Vss+0.4		
	VOLC2	IOL=120 μ A		--	--	0.8xVss		
Input leakage current	ILI			-1	--	1	μ A	See note 6.
Output leakage current	ILO			-3	--	3	μ A	See note 7.
LCD driver ON resistance	Ron	Ta=25 deg. C	V5= -5.0V	--	5	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V5= -3.5V	--	10	50		
Static current dissipation	IDD0	CS = CL = VDD		--	0.05	1	μ A	VDD
Dynamic current dissipation	IDD (1)	During display V5= -5.0V	fCL=2kHz	--	2	5	μ A	VDD See note 12, 13 & 14.
			Rf= 2 MΩ	--	9.5	15		
			fCL= 18kHz	--	5	10		
	IDD (2)	During access tcyc=200kHz		--	300	500	μ A	See note 8.
Input pin capacitance	CIN	Ta= 25 deg. C, f= 1MHz		--	5	8	pF	All input pins
Oscillation frequency	fOSC	Rf= 2.0 MΩ± 2% Vss= -5.0V		15	18	21	kHz	See note 9.
		Rf= 2.0 MΩ± 2% Vss= -3.0V		11	18	21		
Reset time	tR			1	--	1,000	μ S	RES

Notes:

1. Operation over specified voltage range is guaranteed where the supplier voltage change suddenly during the CPU access
2. A0,D0 to D7 E(/RD) R/W(/WR) and CS
3. during continue access at a frequency, the current consumption is adding .

1.6 AC CHARACTERISTIC

MPU Bus Read/Write (8080-family MPU)



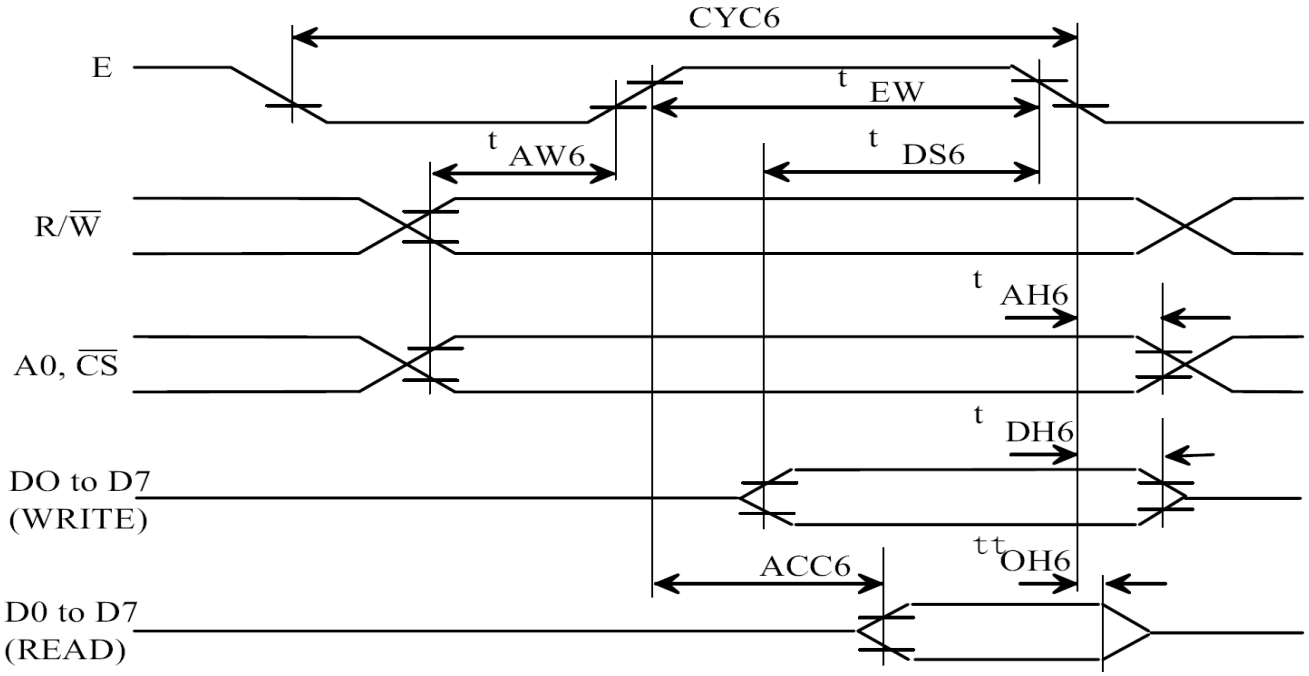
Ta = –10 to 60°C, Vss = 0V 10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			min	max		
Address hold time	tAH8		10	--	ns	A0, CS
Address setup time	tAW8		20	--	ns	
System cycle time	tCYC8		1,000	--	ns	WR, RD
Control pulsewidth	tcc		200	--	ns	
Data setup time	tDS8		80	--	ns	DO to D7
Data hold time	tDH8		10	--	ns	
RD access time	tACC8	CL= 100pF	--	90	ns	
Output disable time	tCH8		10	60	ns	

Note: 1. the parameter increase 250% when the Vdd=3.5V

2. All input and output has a rise or fall time than 20ns.

MPU Bus Read/Write (6800-family MPU)



(VDD = 3.5 to 5.0V, Ta = –10 to +60°C)

Parameter		Symbol	Condition	Rating		Unit	Signal
				min	max		
System cycle time		tCYC6		1,000	--	ns	A0, CS, R/W
Address setup time		tAW6		20	--	ns	
Address hold time		tAH6		10	--	ns	
Data setup time		tDS6		80	--	ns	D0 to D7
Data hold time		tDH6		10	--	ns	
Output disable time		tOH6	CL= 100pF	10	60	ns	
Access time		tACC6		--	90	ns	
Enable pulsewidth	Read	tEW		100	--	ns	E
	Write			8	--	ns	

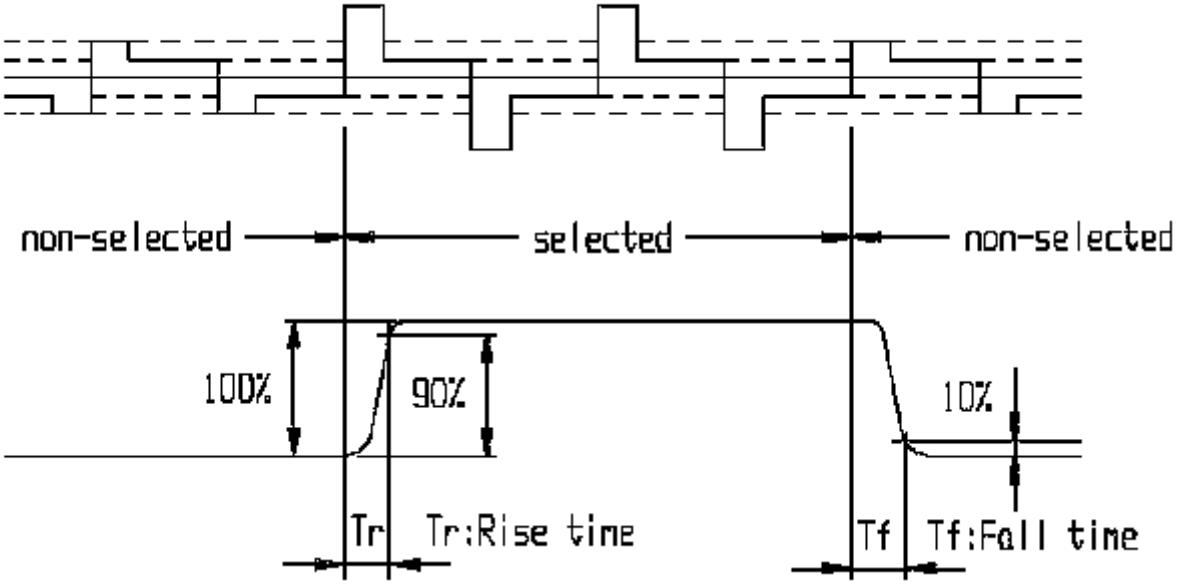
Note: 1. Tcyc6 is the CS cycle time

2. the parameter increase 250% when the Vdd=3.5V

3. . All input and output has a rise or fall time than 20ns.

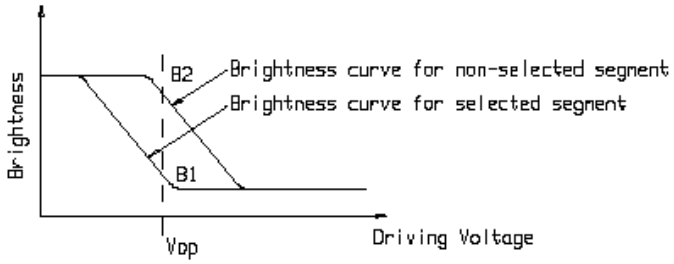
1.7 ELECTRO-OPTICAL CHARACTERISTICS

Note1 : Definition of response time.

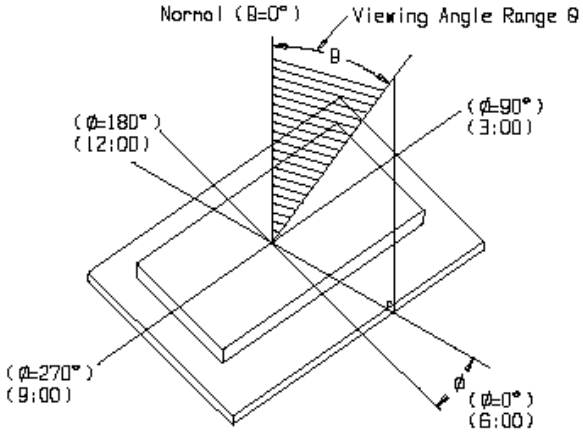


Note2: Definition of contrast ratio 'Cr' .

$$Cr = \frac{\text{Brightness of non-selected segment(B2)}}{\text{Brightness of selected segment(B1)}}$$



Note3: Definition of viewing angle range 'θ'.



1.8 BACKLIGHT CHARACTERISTICS

LCD Module with LED Backlight

ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Item	Symbol	Conditions	Rating	Unit
Absolute maximum forward current	Ifm		180	mA
Peak forward current	Ifp	I msec plus 10% Duty Cycle	540	mA
Reverse voltage	V_r		10	V
Reverse current	I_r		90	uA
Power dissipation	P_d		900	mW
Operating Temperature Range	T_{opr}		-20~+70	℃
Storage Temperature Range	Tstg		-30~+80	℃

ELECTRICAL –OPTICAL CHARACTERISTICS(Ta=25℃,IF=90mA)

COLOR	Wavelength λ p(nm)	Operating Voltage(v)(± 0.15v)	Spectral line half width Δλ(nm)	Forward Current (mA)
Yellow Green	568	4.2	30	90

2. MODULE STRUCTURE

2.1 INTERFACE PIN DESCRIPTION

Pin No.	Symbol	Level	Description
1	VDD	5.0V	Connected to the +5Vdc power. Common to the VCC MPU power pin.
2	VSS	0V	0 Vss pin connected to the system ground.
3	V0	--	Input voltage for LCD,VLCD=VDD-V0
4	/RES	H/L	Reset signal
5	E 1(RD)	H/L	• If the 68-series MPU is connected: Input. Active HIGH. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active LOW. The RD signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status E1: Chip select signal for U1(SEG 0 - 61) E1: Chip select signal for U2(SEG 62 - 122)
6	E 2(RD)	H/L	
7	R/W (WR)	H/L	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is HIGH) or write control signals (if LOW). • If the 80-series MPU is connected: Input. Active LOW. The WR signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of WR signal.
8	A0	H/L	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
9	DB0	H/L	Data bit 0	Three-state I/O. The 8-bit bi-directional data buses to be connected to the 8- or 16-bit standard MPU data buses.
10	DB1	H/L	Data bit 1	
11	DB2	H/L	Data bit 2	
12	DB3	H/L	Data bit 3	
13	DB4	H/L	Data bit 4	
14	DB5	H/L	Data bit 5	
15	DB6	H/L	Data bit 6	
16	DB7	H/L	Data bit 7	
17	A	5.0V	Back light anode
18	K	0V	Back light cathode

2.2 FUNCTION DESCRIPTION

System Bus or MPU interface

1. Selecting an interface type

The S1D15200 series transfers data via 8-bit bi-directional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of HIGH or LOW RES signal level after reset (see Table 1). When the CS signal is high, the S1D15200 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
Active	68-series	↑	↑	↑	↑	↑
Active	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

(1) Data transfer

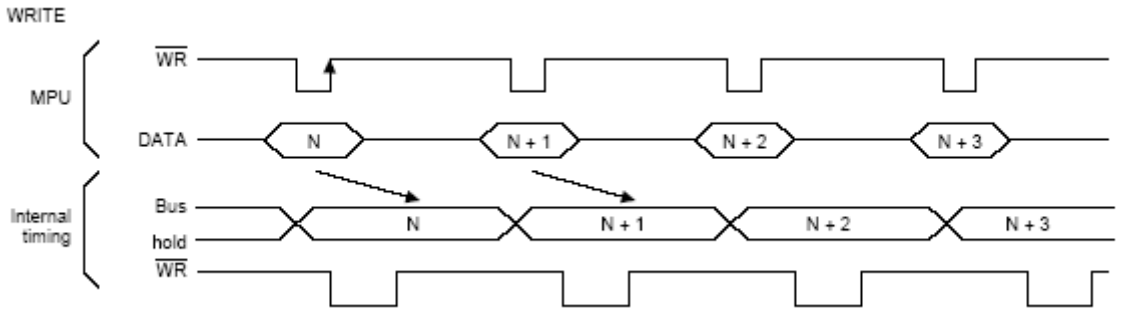
The S1D15200 and S1D15201 drivers use the A0, E (or RD) and R/W (or WR) signals to transfer data between the system MPU and internal registers. The combinations used Access to Display Date RAM and Internal Registers are given in the table blow.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1. No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.



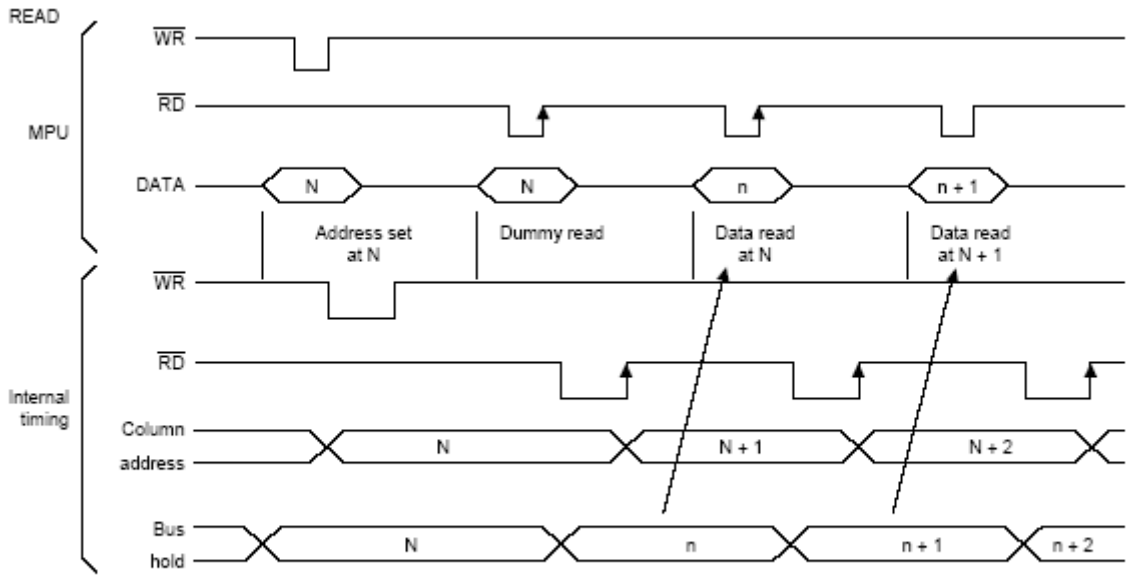


Figure 1 Bus Buffer Delay

(2)Busy flag

When the Busy flag is logical 1, the S1D15200 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and therefore, the MPU processing capacity can greatly be enhanced.

(3) Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

(4) Column Address Counter

The column address counter is a 7-bit presentable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

(5) Page Register

The page resister is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

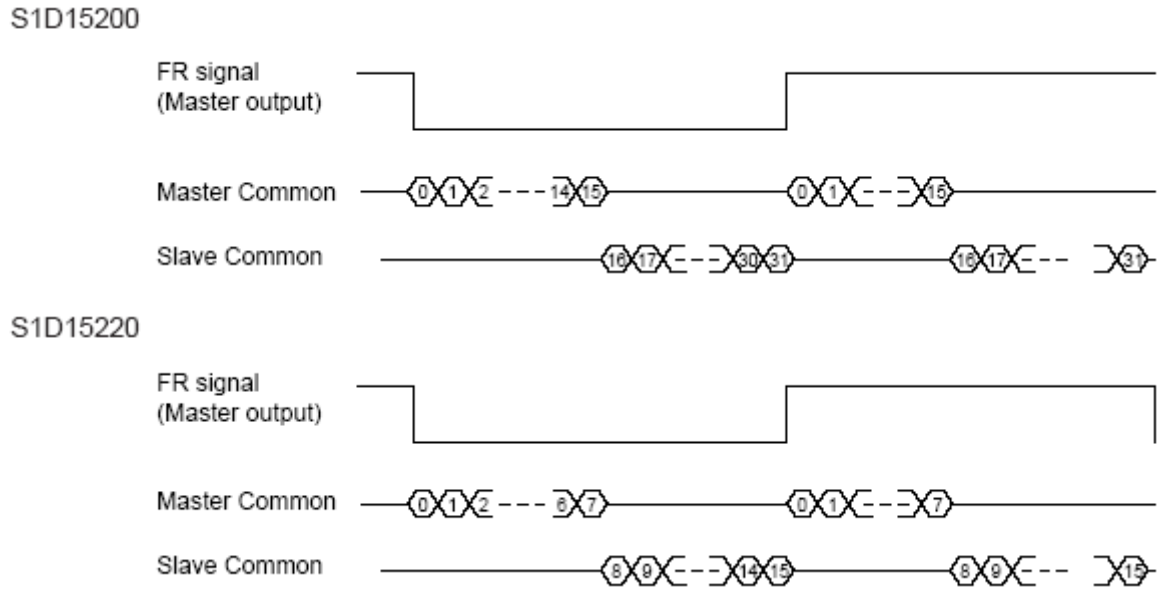
2.3. DISPLAY DATA RAM

(1) Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

(2) Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for S1D15200) or 1/8 or 1/16 duty (for S1D15202) can be selected by the Duty Select command. If the 1/32 duty is selected for the S1D15200 and 1/16 duty is selected for the S1D15202, the 1/32 and 1/16 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.



(3) Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

(4) LCD Driver Circuit

The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

(5) Display Timing Generator

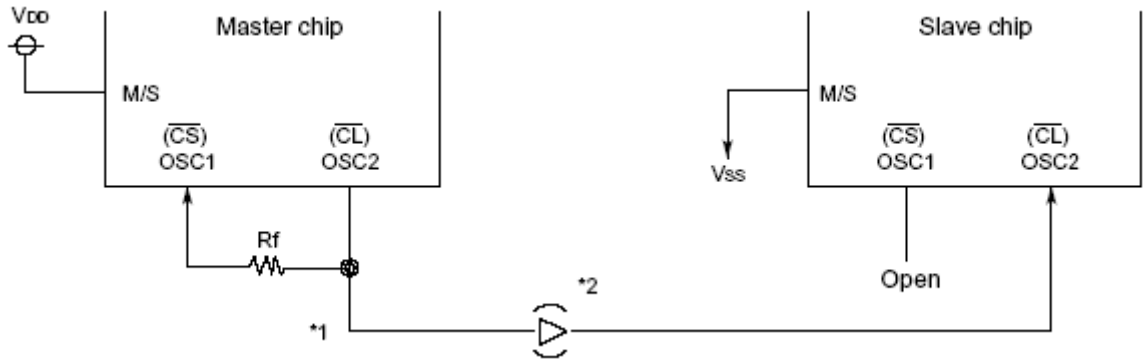
This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate.

CL is used to lock the line counter to the system line scan rate. If a system uses both S1D15200 or S1D15202 and S1D15201 they must have the same CL frequency rating.

(6) Oscillator Circuit (S1D15200*0A Only)

A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of S1D15200 and S1D15202 series models have a built-in oscillator and others use an external clock. This difference must be checked before use. Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, enter the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

• MPU having a built-in oscillator



• MPU driven with an external clock

(7) Reset Circuit

Detects a rising or falling edge of an RES input and initializes the MPU during power-on.

• Initialization status

1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 3.
6. 1/32 duty (S1D15200) or 1/16 duty (S1D15202) is selected.
7. Forward ADC is selected (ADC command D0 is1 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at RES pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 0-series MPU, the RES input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered. As shown for the MPU interface (reference example), the RES pin must be connected to the Reset pin and reset at the same time as the MPU initialization. If the MPU is not initialized by the use of RES pin during power-on, an unrecoverable MPU failure may occur. When the Reset command is issued, initialization

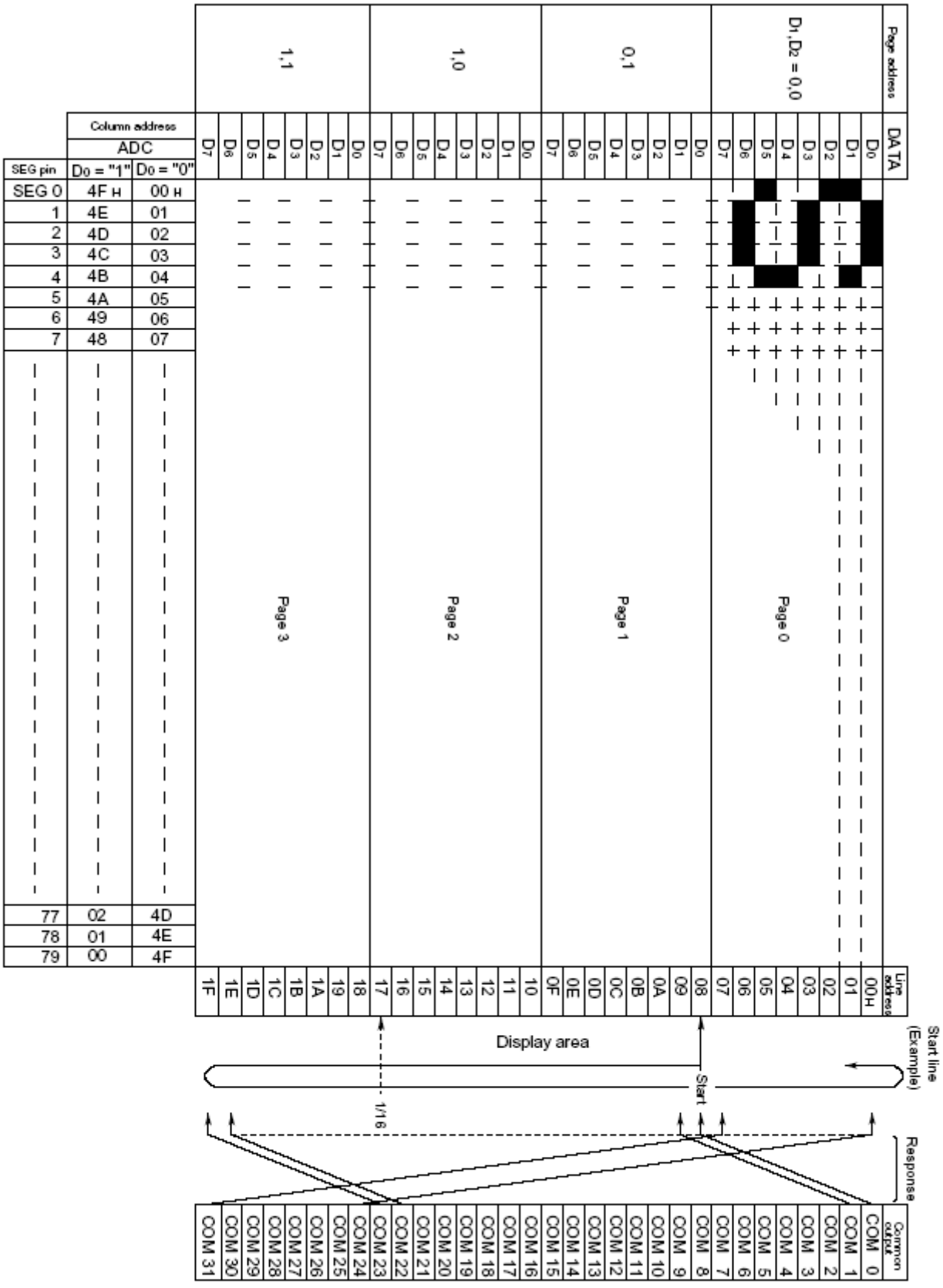


Figure 2 Display Data RAM Addressing

1/5 bias, 1/16 duty
1/6 bias, 1/32 duty

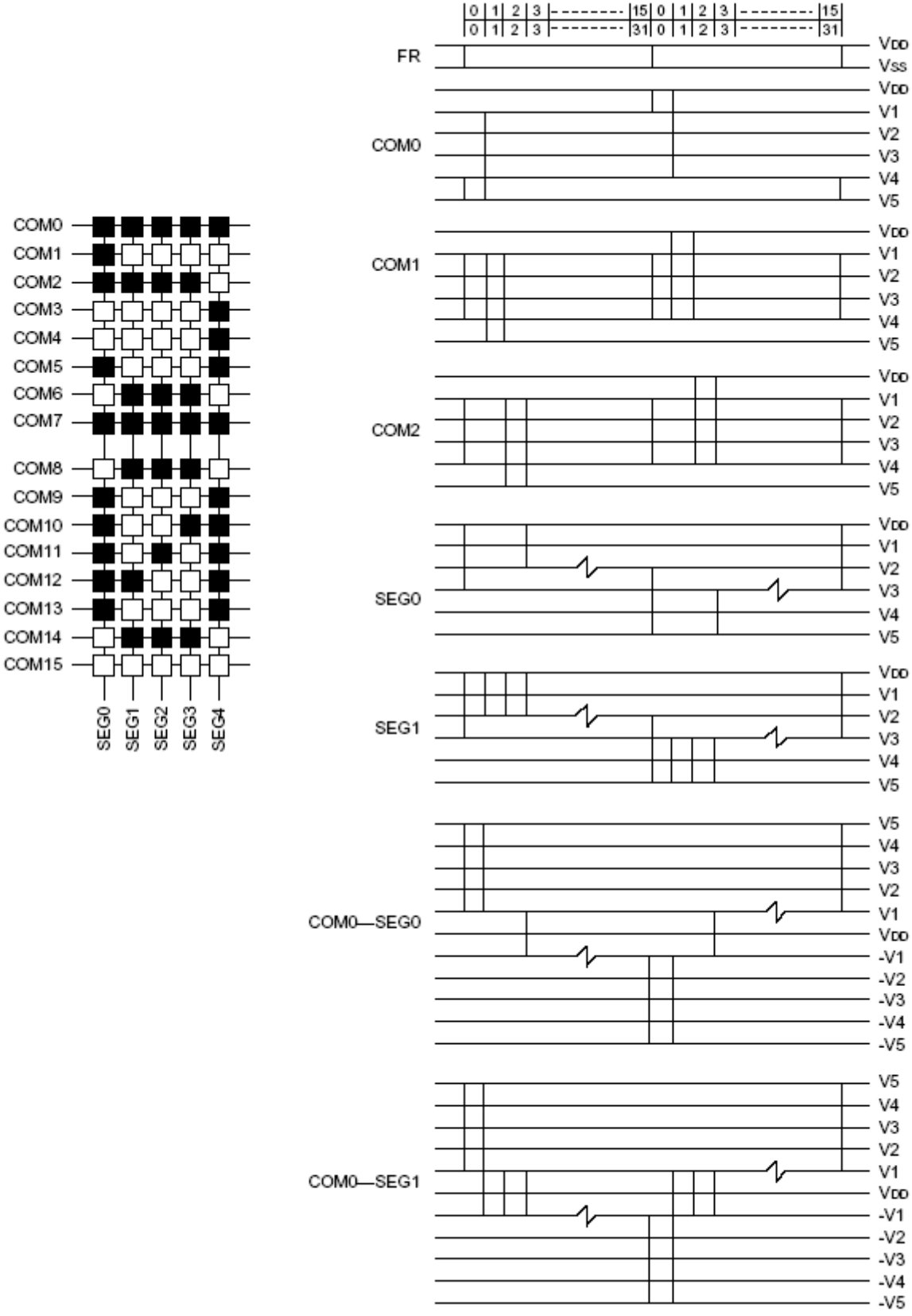


Figure 4 LCD drive waveforms example

2.4. COMMAND TABLE

Table 3

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(1) Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
(2) Display start line	0	1	0	1	1	0Display start address (0 to 31)						Specifies RAM line corresponding to top line of display.
(3) Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
(4) Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
(5) Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
(6) Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
(7) Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
(8) Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
(9) Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
(10) Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
(11) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
(12) End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
(13) Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

2.5 COMMAND DESCRIPTION

Command Description

Table 3 is the command table. The S1D15200 series identifies a data bus using a combination of A0 and R/W (RD or WR)signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

(1) Display ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

• D=1: Display ON

• D=0: Display OFF

(2) Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

(3) Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified.The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

(4) Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

(5) Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

• The busy bit indicates whether the driver will accept a command or not.

Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.

Busy=0: The driver will accept a new command.

• The ADC bit indicates the way column addresses are assigned to segment drivers.

ADC=1: Normal. Column address n ® segment driver n.

ADC=0: Inverted. Column address 79-u ® segment driver u.

• The ON/OFF bit indicates the current status of the display.

It is the inverse of the polarity of the display ON/OFF command.

ON/OFF=1: Display OFF

ON/OFF=0: Display ON

• The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

RESET=1: Currently executing reset command.

RESET=0: Normal operation

6) Write Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

(7) Read Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ¬ column address 4FH, … (inverted)
D=0: SEG0 ¬ column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

(9) Static Drive ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on D=0: Static drive off

(10) Select Duty

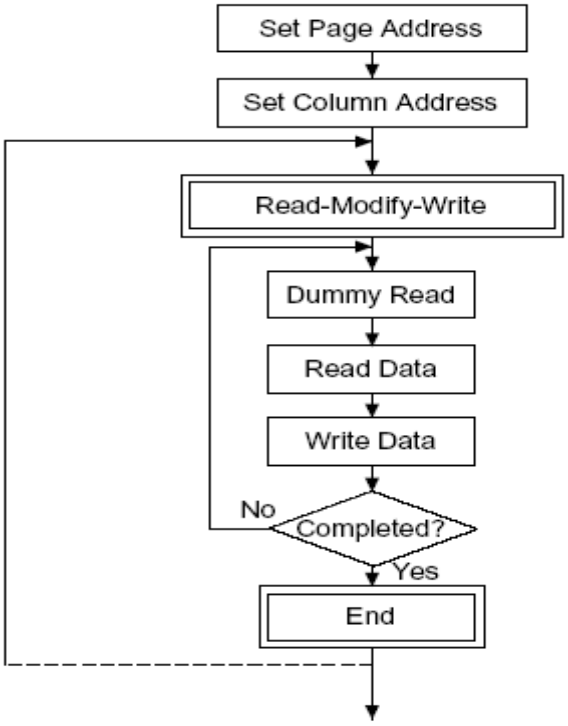
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the S1D15200F and S1D15202F. It is invalid for the S1D15201F which performs passive operation. The duty cycle of the S1D15201F is determined by the externally generated FR signal.
D=1: 1/32 duty cycle 1/16 duty cycle
D=0: 1/16 duty cycle 1/8 duty cycle

(11) Read-Modify-Write

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

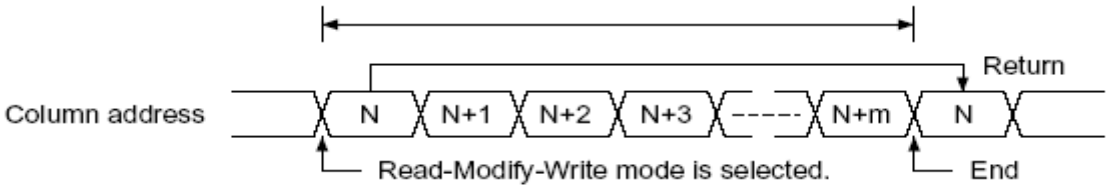
This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.
• Operation sequence during cursor display
When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



(12) End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



(13) Reset

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears

• the display start line register.

• and set page address register to 3 page.

It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the RES pin. The Reset command cannot be used instead of this Reset signal.

(14) Power Save (Combination command)

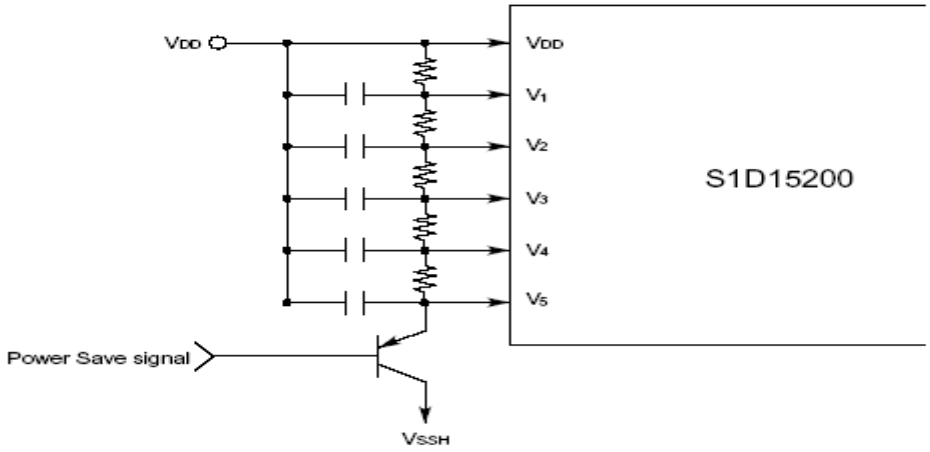
The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:

(a) The LCD drive is stopped, and the segment and common driver outputs are set to the VDD level.

(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.

(c) The display and operation modes are kept.

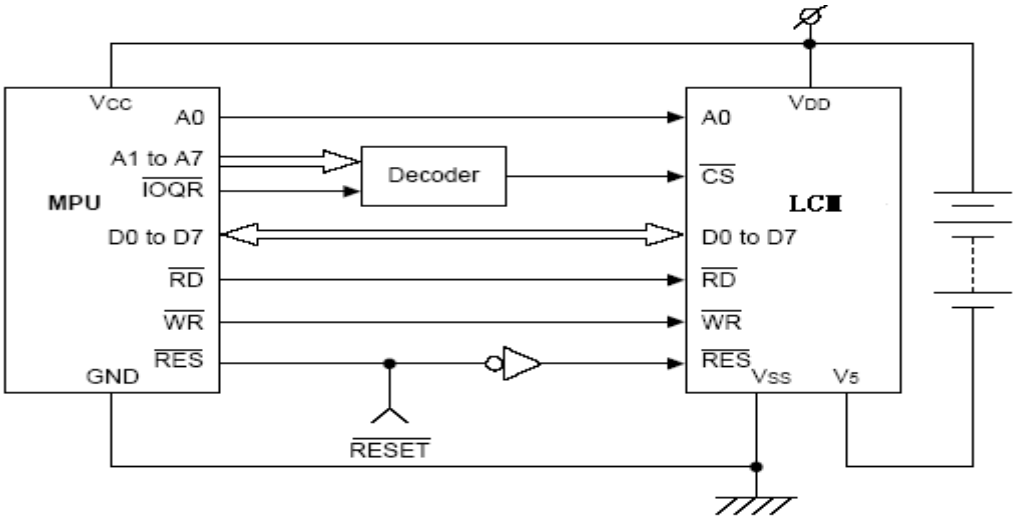
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



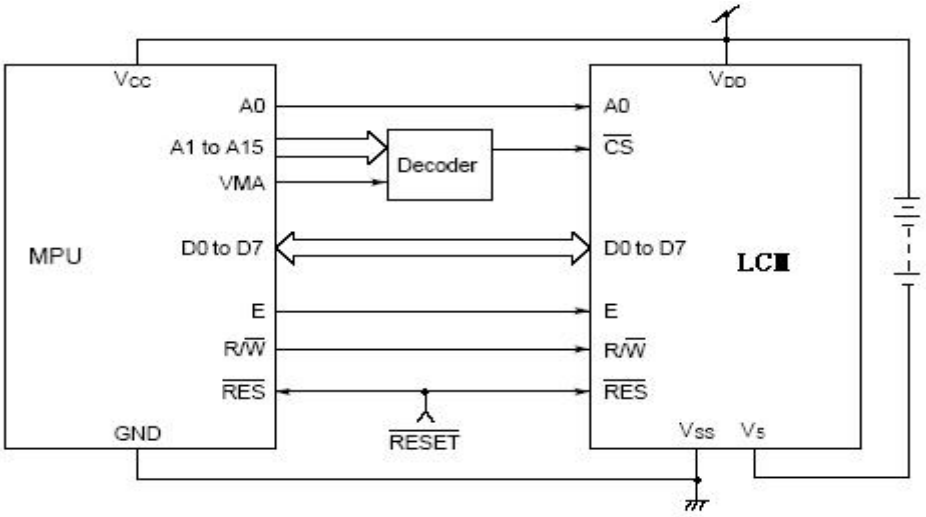
If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affectedand reduce the power consumption using the divider resistor.

2.6 MPU INTERFACE CONFIGURATION

80 Family MPU

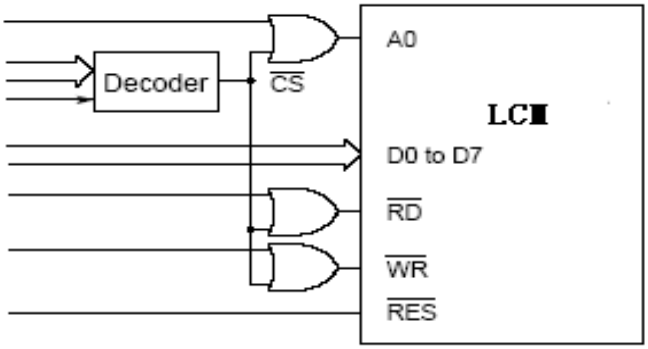


68 Family MPU (Reference)



Refer to the figure above as to LCM

*TG12232D(internal oscillating) does not have CS terminal. Input OR output with CS signal to AD. RD(E),WR(R/W)terminals as the figure below.



3. RELIABILITY TEST AND QUALITY

3.1. RELIABILITY TEST CONDITION

No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	60 °C 200 hrs	------
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-10 °C 200 hrs	------
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50 °C 200 hrs	------
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	0 °C 200 hrs	------
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. -10°C 30min ⇌ 25°C 5min. ⇌ 60°C 30min 1 cycle	-10°C / 60°C 10 cycles	------

Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25° C

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	MIL-202E-213B
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	MIL-202E-105C
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	MIL-883B-3015.1

Failure Judgment criterion

Criterion Item	Test Item No.											Failure Judgment Criterion
	1	2	3	4	5	6	7	8	9	10	11	
Basic specification												Out of the Basic specification
Electrical characteristic												Out of the DC and AC characteristic
Mechanical characteristic												Out of the Mechanical specification Color change: out of Limit Appearance Specification
Optical characteristic												Out of the Appearance Standard

3.2. QUALITY GURANTEE

Acceptable Quality Level, Each lot should satisfy the quality level defined as follows.
-Inspection method: MIL-STD-105E LEVEL II Normal one time sampling

AQL

Partition	AQL	Description
A: Major	0.4%	Functional defective product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

Definition of 'LOT'

One lot means the delivery quality to customer at once time.

Conditions of Cosmetic Inspection

. Environmental condition

The inspection should be performed at the 1metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

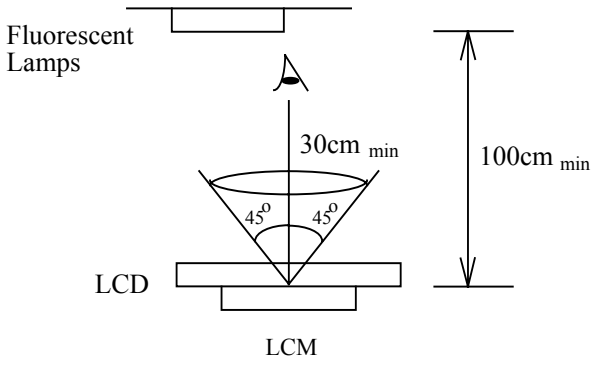
Driving voltage

The Vo value which the most optimal contrast can be obtained near the specified Vo in the specification (Within of the typical value at 25℃.).

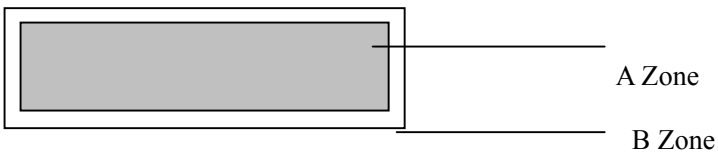
3.3. INSPECTION METHOD

The visual check should be performed vertically at more than 30cm distance from the LCD panel

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:

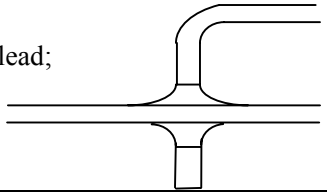
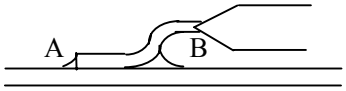
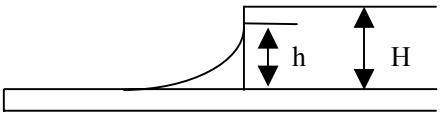


A Zone: Active display area (minimum viewing area).

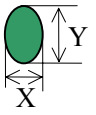
B Zone: Non-active display area (outside viewing area).

3.4. INSPECTION STANDARD FOR SOLDER

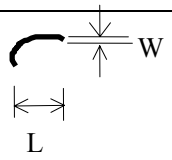
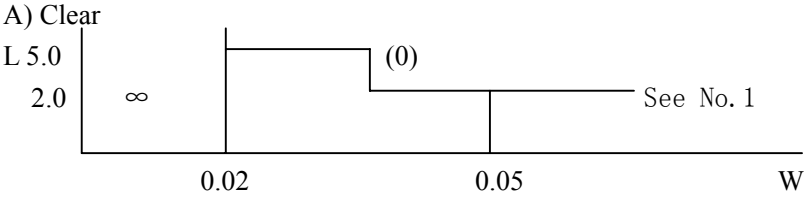
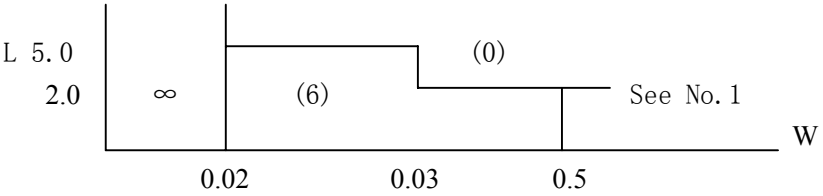
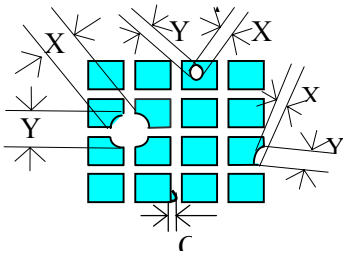
Module Cosmetic Criteria

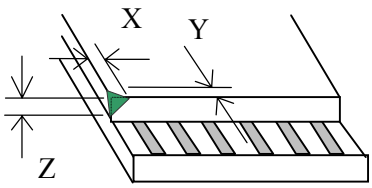
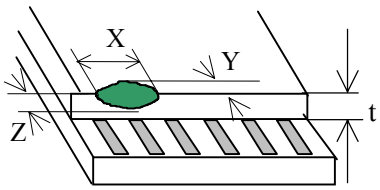
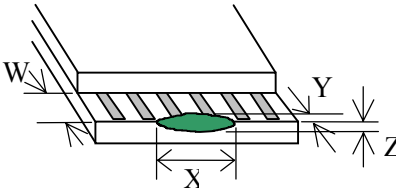
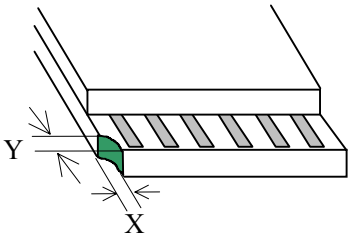
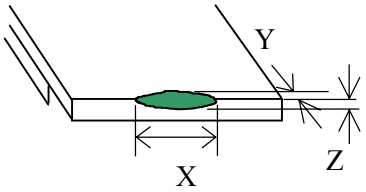
No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern Peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (Φ0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed Φ0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Plate discoloring 1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead; Solder should not hide the lead form perfectly too much 	Minor
	2. Flat packages	Either "toe"(A) or "heal' (B) of The lead to be covered by 'Filet' Lead form to be assume over Solder. 	Minor
	3. Chips	(3/2) H ≥h ≥ (1/2) H 	Minor

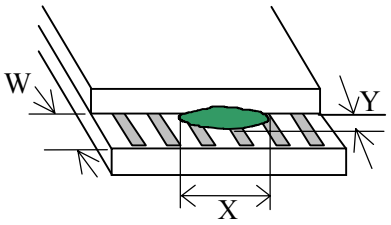
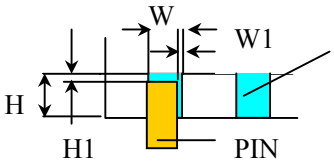
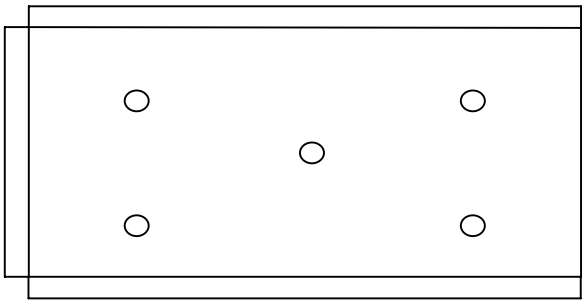
3.5. SCREEN COSMETIC CRITERIA (APPEARANCE)

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="8">1</td><td>Short or open circuit</td><td rowspan="8">No allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td>Wrong or missing component</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect (dim, ghost)</td><td rowspan="2">Refer to the approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect, Black spot, dust (including Polarizer)
Φ=(X+Y)/2</td><td> 

<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.20</td><td>6</td></tr>
<tr><td>0.20<ϕ≤0.3</td><td>2</td></tr>
<tr><td>ϕ>0.30</td><td>0</td></tr>
</table></td></tr>
</table>

No.	Item	Criterion
4	Line defect, Scratch: In accordance with spots and lines operating cosmetic criteria. When the light reflective on the panel surface, the scratches are not to be remarkable.	 Line / Acceptable Qty. L / W --- / 0.015≧W / Disregard 3.0≧L / 0.03≧W / 2 2.0≧L / 0.05≧W 1.0≧L / 0.1＞W / 1 --- / 0.05<W / Applied as point defect Unit: mm A) Clear  Note: ( ) –Acceptable Qty in active area L –Length (mm) W –Width (mm) ∞ –Disregard B) Unclear 
5	Rainbow	Not more than two colors change across the viewing area
6	Dot-matrix pattern ϕ = (X+Y)/2	Pin hole:  Size / Acceptable Qty. ϕ＜0.1 / Disregard 0.10≦ϕ≦0.20 / 1 ϕ>0.20 / 0 C: Shall not touch other dot(s).

No.	Item	Criterion
7	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width	 Acceptable criterion X: ≤2 ; Y: 0.5mm ; Z: ≤t  Acceptable criterion X: ≤2 ; Y: 0.5mm ; Z: ≤t/2  Acceptable criterion X: Disregard ; Y: ≤0.2 ; Z: ≤t  Acceptable criterion X: ≤3 ; Y: ≤2 ; Z: ≤t shall not reach to ITO  Acceptable criterion X: ≤5 ; Y: ≤2 ; Z: ≤t/3

No.	Item	Criterion
8	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.
9	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
10	PIN	Position  W1≤1/3W H1≤1/3H
11	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX/BMIN≤2 -BMAX : Max. value by measure in 5 points -BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure 
12	Allowable density	Above defects should be separated more than 10mm each other.
13	Rubbing line	Not to be noticeable.
14	Dot size	To be 95% ~ 105% of the dot size (typ.) in drawing, Partial defects of each dot (ex. Pin-hole) shold be t4reated as 'spot'.(see Screen Cosmetic Criteria (operating) No.)

No.	Item	Criterion	
15	Bubbles in polarizer	Size : d mm	Acceptable Qty in active area
		d≦0.3	Disregard
		0.3<d≦1.0	3
		1.0<d≦1.5	1
		1.5<d	0
16	Allowable density	Above defects should be seated more than 30mm each other	
17	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Backlit type should be judged with back-lit on state only.	
18	Contamination	Not to be noticeable.	

Note:
'Clear'= the shade and size are not changed by Vo.
'Unclear'= the shade and size are changed by V0.
Size: d=(long length + short length)/2
The limit samples for each item have priority
Complete defects are defined item by item, but if the number of defects is defined in above table, the total number should not exceed 10.
In case of ' concentration', even the spots or the lines of 'disregarded size should not allowed. Following three situations Should be treated as 'concentration'.
-7 or over defects in circle of Φ2mm
-10 or over defects in circle of Φ10㎜
-20 or over defects in circle of Φ20㎜

3.6. PRECAUTION FOR USING LCM MODULE

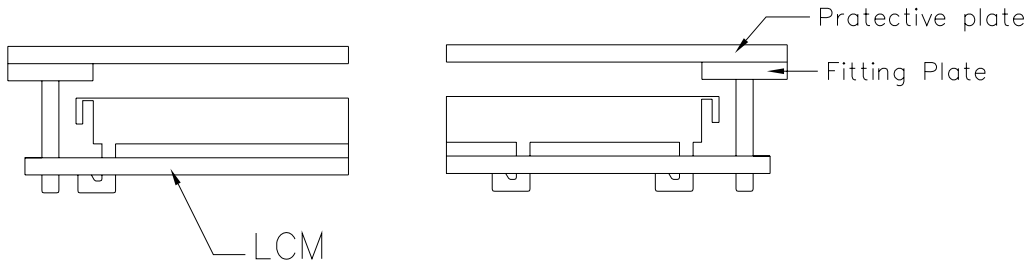
LCD is composed of glass and polarizer. Pay attention to the following items when handing.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or Polarizer peel-off may occur with high humidity.
(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB Pencil lead (Glass, tweezers, etc.).
(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic, substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.
(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum Do not scrub hard to avoid damaging the display surface.
(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
(6) Avoid contacting oil and fats.
(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature the must be warmed up in a container before coming is contacting temperature air.
(8) Do not put or attach anything on the display area to avoid leaving marks on.
(9) Do not touch the display with bare hands. This will stain the display and degrade insulation between terminals (some cosmetics are determinated to the polarizers).
(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

3.7. INSTALLING LCM MODULE

The hole in the printed circuit board is used to if LCM as shown in the picture below. Attend to the following items when installing the LCM

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm]

3.8. PRECAUTION FOR HANDING LCM MODULE

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change shape of the tab on the metal frame
(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
(3) Do not damage or modify the pattern writing on the printed circuit board.
(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
(6) Do not drop, bend or twist LCM

3.9. Electro-Static DISCHARGE CONTROL

Since this module uses a CMOS LSI, the same attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.
(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
(5) As far as possible make the electric potential of your work clothes and that of the workbench the ground potential.
(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

3.10. PRECAUTION FOR SOLDERING TO THE LCM

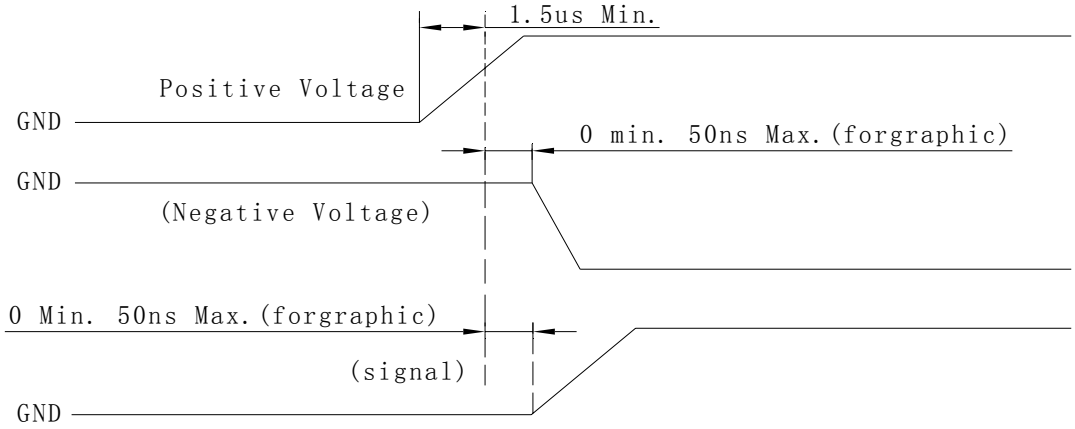
(1) Observe the following when soldering lead wire , connector cable and etc. to the LCM
-Soldering iron temperature: 280℃±10℃
-Soldering time: 3-4 seconds
-Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation.(This does not apply in the case of non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electro-luminescent panel and PC board, the panel and board should not be detached more than three times, This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
(3) When remove the electro-luminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PX board could be damaged.

3.11. PRECAUTIONS FOR OPERATION

(1) Viewing angle varies with the change of liquid crystal driving voltage (V0). Adjust Vo to show the best contrast.
(2) Driving the LCD in the voltage above the limit shortens its life.
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD cell be out of the order. It will recover when it returns to the specified temperature range.
(4) If the display area is pushed hard during operation, the display will become abnormal, however, it will return to normal. If it is turned off and then back on. Used under the relative condition of 40℃, 50%RH.
(5) When turning the power on input each signal after the positive/negative voltage becomes stable.



3.12. STORAGE

When storing LCD as spares for some years, the following precautions are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0℃ and 35℃

(3) The polarizer surface should not come in contact with any other object.(we advise you to store them in the container in which they were shipped.)

(4) Environmental conditions:

-Don not leave them for more than 168hrs. at 60℃

-Should not be left for more than 48hrs. at -20℃.

3.13. SAFETY

(1) It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2)If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.