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The LCD(M) Specialist

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PART NO. : PRG1203B-SERIES

FOR MESSRS. : _____

CONTENTS

龐誼科技
93.03.23
發行

ACCEPTED BY : _____ PROPOSED BY : _____

RECORD OF REVISION

DATE	PAGE	SUMMARY

1. General description

PRG1203B is a graphic LCM ,it includes row driver/line driver、122X32 pixels LCD .It can display graphic picture and English text ,also can show 7X2 (16X16 pixels)Chinese words.

Main Electronic parameter & capability:

a. Power: VDD: +5V ；
b. Display panel: 122(line)X32(row) pixels;
c. Interface fit drive timing of 8080 series & 68000 series MPU
d. Drive mode: 1/32 duty, 1/5 bias;
e. Operating temperature: 0°C □ +50°C; Storage temperature: -10°C □ +60°C
f. Module can mount LED backlight
g. LCD panel 6 O ’ clock, STN.

2. Maximum absolute limit

Characteristics	Symbol	Ratings	Remark
Operating Voltage	VDD-VSS	-0.3V to +7.0V	
Driver Supply Voltage	V5-VDD	-3V to -13V	
Input Voltage Range	VIN	-0.3V to VDD + 0.3V	
Operating Temperature	TA1	-10°C to+60°C	Normal temperature LCM
	Ta2	-20°C to+60°C	Wide temperature LCM
Storage Temperature	Tsto	-25°C to+70°C	

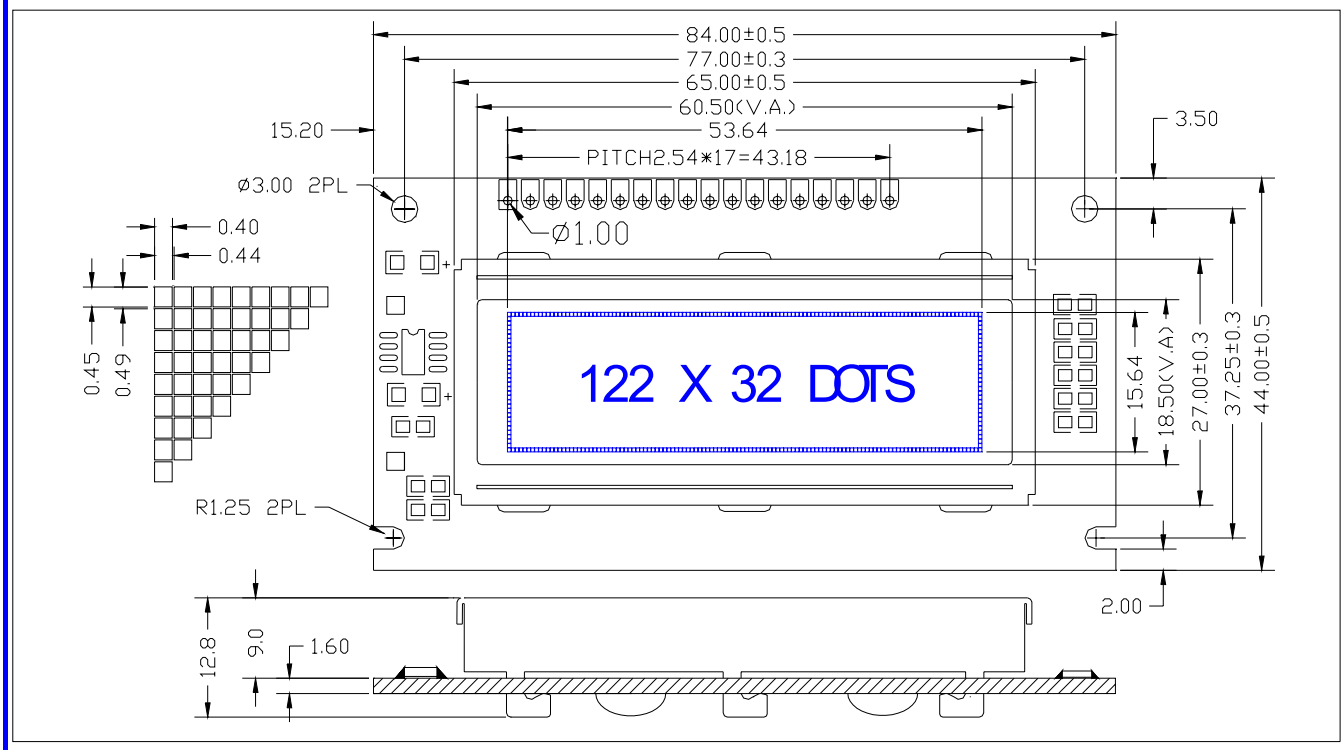
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device.

3. Mechanical characteristics

a) Physical data

ITEM	Standard value	Unit	Remark
Dot Pixels	122X32	Dots	
Module Size	84.00X44.0X12.8	mm	
Viewing Area	60.50X18.50	mm	
Active Area	53.64X15.64	mm	
Dot Size	0.40X0.45	mm	
Dot Pith	0.44X0.49	mm	
Approx. weight	35.7	g	
Drive method	8-bits Parallel data input		

b) External dimensions



4. Electrical characteristics

DC characteristics

Ta = 0 to 50 deg. C, vdd = 0 V unless stated otherwise

Parameter		Symbol	Condition	Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating voltage (1)	Recommended	Vss		-5.5	-5.0	-4.5	V	Vss
	Allowable			-7.0	—	-2.4		
Operating voltage (2)	Recommended	V5		-13.0	—	-3.5	V	V5 See note 10.
	Allowable			-13.0	—	—		
	Allowable	V1,V2		0.6Xv5	—	vdd	V	V1,V2
	Allowable	V3,V4		V5	—	0.4xV5	V	V3,V4
High-level input voltage		VIHT		Vss+2.0	—	Vdd	V	note 2 & 3.
		VIHC		0.2xVss	—	Vdd		
		VIHT	Vss = -3 V	0.2xVss	—	Vdd		note 2 & 3
		VIHC	Vss = -3 V	0.2xVss	—	Vdd		
Low-level input voltage		VILT		VSS		Vss+0.8		note 2 & 3.
		VILC		Vss		0.8xVss		
		VILT	Vss = -3 V	Vss		0.85xVss		note 2 & 3,
		VILC	Vss = -3 V	Vss		0.8xVss		
High-level output voltage		voht	ioh = -3.0 mA	Vss+2.4	—	—	V	note 4 & 5. osc2
		VOHC1	ioh = -2.0 mA	Vss+2.4	—	—		
		VOHC2	IOH=-120uA	0.2xVss	—	—		
		Voht	Vss = -3 V ioh = -2 mA	0.2xVss			V	note 4 & 5. OSC2
		VOHC1	Vss = -3 V ioh = -2 mA	0.2xVss				
		VOHC2	Vss = -3 V ioh = -50uA	0.2xVss				
Low-level output voltage		volt	iol = 3.0 mA	—	—	Vss+0.4	V	note 4 & 5. OSC2
		VOLC1	iol = 2.0 mA	—	—	Vss+0.4		
		VOLC2	IOL=120uA	—	—	0.8xVss		
		VOLT	Vss = -3 V iol = 2 mA			0.8xVss	V	note 4 & 5. OSC2
		VOLC1	Vss = -3 V iol = 2 mA			0.8xVss		
		VOLC2	VSS = -3 V iol = 50 uA			0.8xVss		
Input leakage current		ILI		-1.0	—	1.0	uA	note 6.

Output leakage current	ILO			-3.0	—	3.0	uA	note 7.
LCD driver ON resistance	ron	Ta =25℃	V5=-5.0V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to15, note 11
			V5 = -3.5 V	—	10.0	50.0		
Static current dissipation	iddq	CS = CL = vdd		—	0.05	1.0	uA	vdd
Dynamic current dissipation	IDD(1)	V5 =-5.0V	fCL=2kHz	—	2.0	5.0	uA	vdd note 12, 13&14.
			Rf = 1 MΩ	—	9.5	15.0		
			fCL=18kHz	—	5.0	10.0		
		V5 =-5V Vss = -3 V	fCL=2kHz		1.5	4.5	uA	vdd note 12 & 13.
			Rf=1MΩ		6.0	12.0		
	IDD (2)	During access tcyc=200 kHz		—	300	500	uA	note 8.
		Vss =-3V, tcyc = 200 kHz			150	300		
Input pin capacitance	Cin	Ta=25℃ f=1MHz		—	5.0	8.0	PF	All input pins
Oscillation frequency	fosc	Rf=1.0MΩ±2% Vss=-5.0V		15	18	21	kHz	note 9.
		Rf=1.0MΩ±2%, Vss = -3.0 V		11	16	21		
Reset time	tR			1.0	—		uS	RES note15

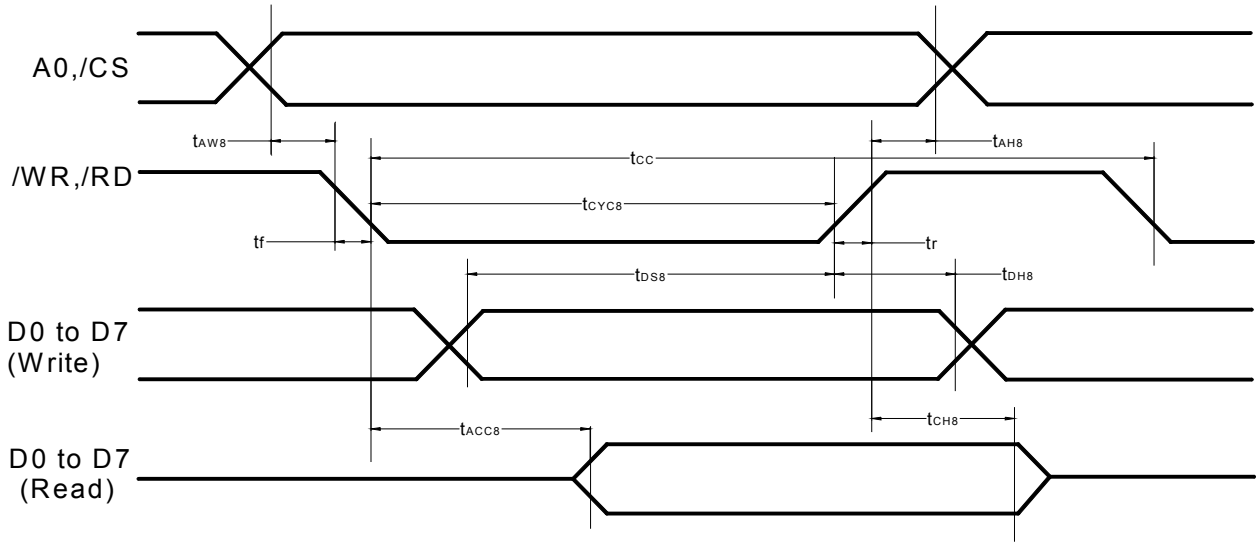
Notes:

1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access
2. A0, DO to D7, E (or RD), R/W (or WR) and CS
3. CL, FR, M/S and RES
4. D0 to D7
5. FR
6. AO, E (or RD), R/W (or WR), CS, CL, M/S and RES
7. When DO to D7 and FR are high impedance.
8. During continual write access at a frequency of tcyc. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V1…V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. SED1520FAA only. Does not include transient currents due to stray and panel capacitances.
13. SED1520F0A only. Does not include transient currents due to stray and panel capacitances.
14. SED1521*0* only. Does not include transient currents due to stray and panel capacitances.
15. tR (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the SED1520 series enters the normal operation status after this tR

b.1) AC CHARACTERISTICS

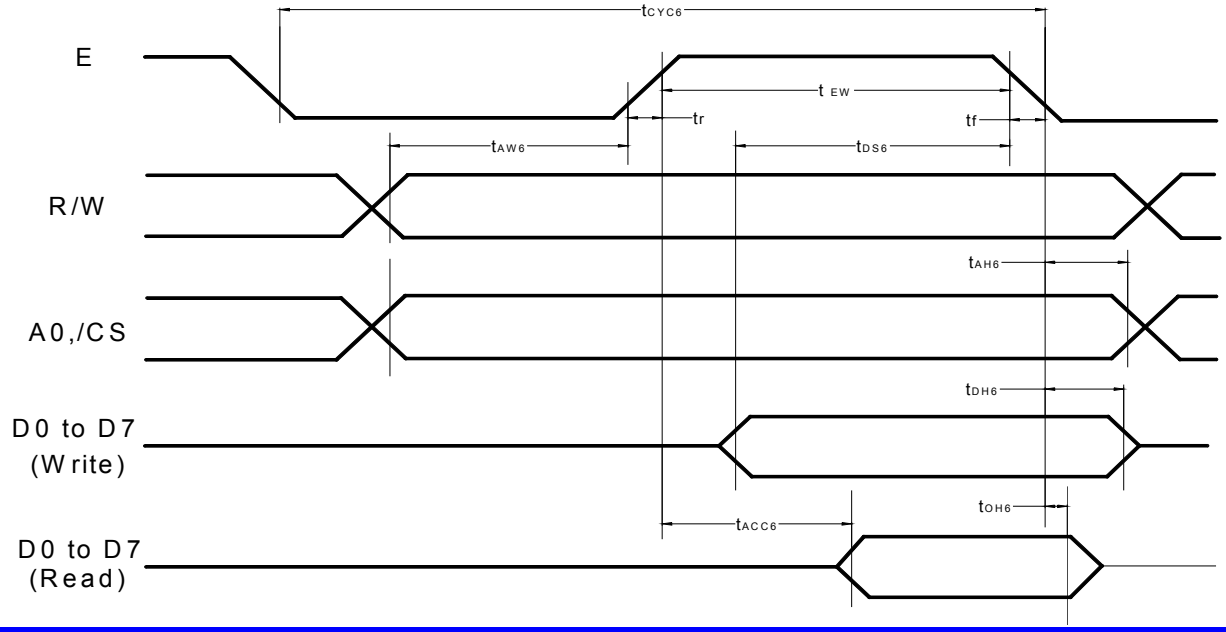
MPU Bus Read/Write Ⅰ (8080 family MPU) (ta = 25°C, VDD = 5.0V)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8		10	—	ns	AO,CS
Address setup time	tAW8		20	—	ns	
System cycle time	Tcyc8		1000	—	ns	WR,RD
Control pulse width	tec		200	—	ns	
Data setup time	tDS8		80	—	ns	DO to D7
Data hold time	tDH8		10	—	ns	
RD access time	TACC8	CL=100pF	—	90	ns	
Output disable time	tCH8		10	60	ns	
Rise and fall time	tr,tf	—	—	15	ns	—



MPU Bus Read/Write II (68 family MPU) (Vdd = 5.0 V, Ta = -20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8	—	20	—	ns	AO,CS
Address setup time	tAW8		40	—	ns	
System cycle time	tCYC8		2000	—	ns	WR,RD
Control pulse width	tec		400	—	ns	
Data setup time	tDS8	—	160	—	ns	DO to D7
Data hold time	tDH8		20	—	ns	
RD access time	tACC8	CL=100pF	—	180	ns	
Output disable time	tCH8		20	120	ns	
Rise and fall time	tr.tf	—	—	15	ns	—



C) LED Backlight

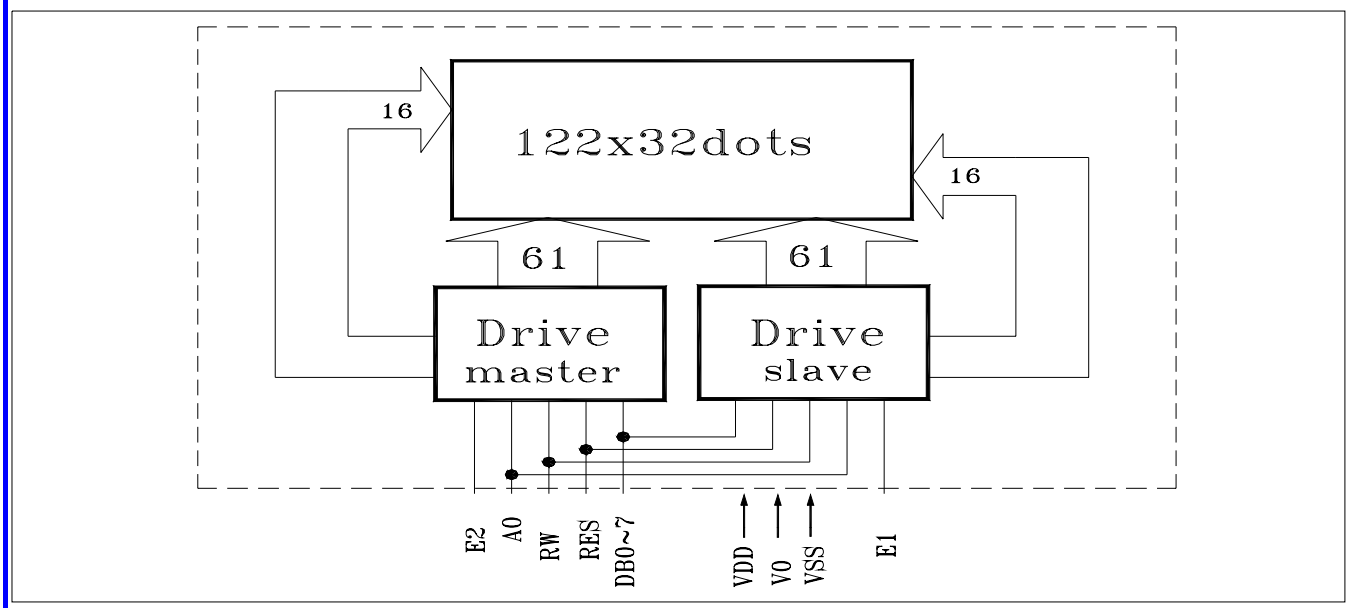
Item	Unit	Standard value			Condition
		Min.	Typ	Max.	
Supply voltage	V	3.9	4.2	4.5	
Initial brightness	cd/cm^2		60		
Life time	Hours	10000			
Current	mA		100		
Luminous color	—	Yellow-green			
Operating Temp.	℃	-15		70	
Storage Temp.	℃	-25		80	

5.Operating Principles

a)Pin description

Pin no	Symbol	Level	Function
1	VSS	0V	GND
2	VDD	+5V	Power Supply
3	V0	-	Power Supply for LCD
4	A0	H/L	Select Data or Instruction
5	E1		enable1 (SLAVE)
6	E2		enable2 (MASTER)
7	R/W	H/L	Read or Write signal
8~15	DB0~DB7	H/L	DATA BUS
16	RET	H/L	RESET signal
17	BLA	+4.2V	For Backlight voltage
18	BLK	0V	

b) Block Diagram



6. Operating Methods

a) Input data and control signal

Command	Code											Function
	AO	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
Display *On/OFF*	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column address	0	1	0	0	Column address (0 to 60)							Sets display RAM column address in column address register.
Read status	0	0	1	BUSy	ADC	ON/OFF	RES	0	0	0	0	Reads the following status: BUSY :1: Busy 0: Ready ADC: 1; CW output 0: CCW output ON/OFF 1: Display off 0: Display on RES 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	*Read data*								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output. 1: CCW output
Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD duty cycle 1: 1/32 0: 1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

b) Command Description

Display ON/OFF

A0		R/W	D7	D6	D5	D4	D3	D2	D1	Do
0	1	0	1	0	1	0	1	1	1	D

This command turns the display on and off.
D=1: Display ON D=0: Display OFF

Display Start Line

0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	0	A4	A3	A2	A1	A0

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used. This command loads the display start line register

A4	A3	A2	A1	Ao	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
~	~	~	~	~	~
1	1	1	1	1	31

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	0	1	1	1	0	A1	A0

This command loads the page address register.

A0	0	1	0	1
A1	0	0	1	1
Page	0	1	2	3

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
1	0	0	1	1	1	1	79

Read Status

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

• The busy bit indicates whether the driver will accept a command or not.
Busy=1 The driver is currently executing a command or is resetting. No new command will be accepted.
Busy=0: The driver will accept a new command.

• The ADC bit indicates the way column addresses are assigned to segment drivers. ADC=1: Normal. Column address n —> segment driver n. ADC=0: Inverted- Column address 79-u -^ segment driver u.

• The ON/OFF bit indicates the current status of the display. It is the inverse of the polarity of the display ON/OFF command. ON/OFF=1: Display OFF ON/OFF=0: Display ON

• The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode. RESET=1: Currently executing reset command. RESET=0: Normal operation.

Write Display Data

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of me column address and page address registers and then increments the column address register by one

Read Display Data

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register. After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	0	1	0	0	0	0	D

This command selects the relationship between display data RAM column addresses and segment drivers.
D= 1: SEG0 <— column address 4FH, -.. (inverted)
D= 0: SEG0 <--- column address 00H, ... (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D

Static Drive ON/OFF

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	0	1	0	0	1	0	D

Forces display on and all common outputs to be selected. D= 1: Static drive on D=0: Static drive off

Select Duty

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	0	1	0	1	0	0	D

This command sets the duty cycle of the LCD drive and is only valid for the SED1520F . It is invalid for the SED1521F which performs passive operation. The duty cycle of the SED1521F is determined by the externally generated FR signal.
D=I: 1/32 duty cycle 1/16 duty cycle
D=0: 1/16 duty cycle 1/8 duty cycle

Read-Modify-Write

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	1	0	0	0	0	0

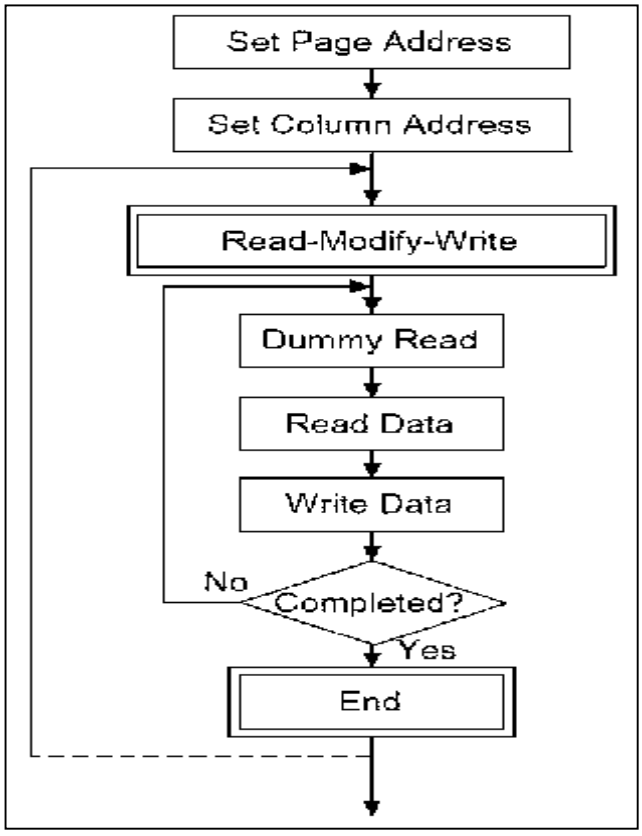
This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.
Operation sequence during cursor display
When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).
Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.

End

A0		R/W	D7	D6	D5	D4	D3	D2	D1	D0
	RD	WR								
0	1	0	1	1	1	0	1	1	1	0

This command cancels read-modify-write mode and restores the contents of the column address register to their

value prior to the receipt of the Read-Modify-Write command



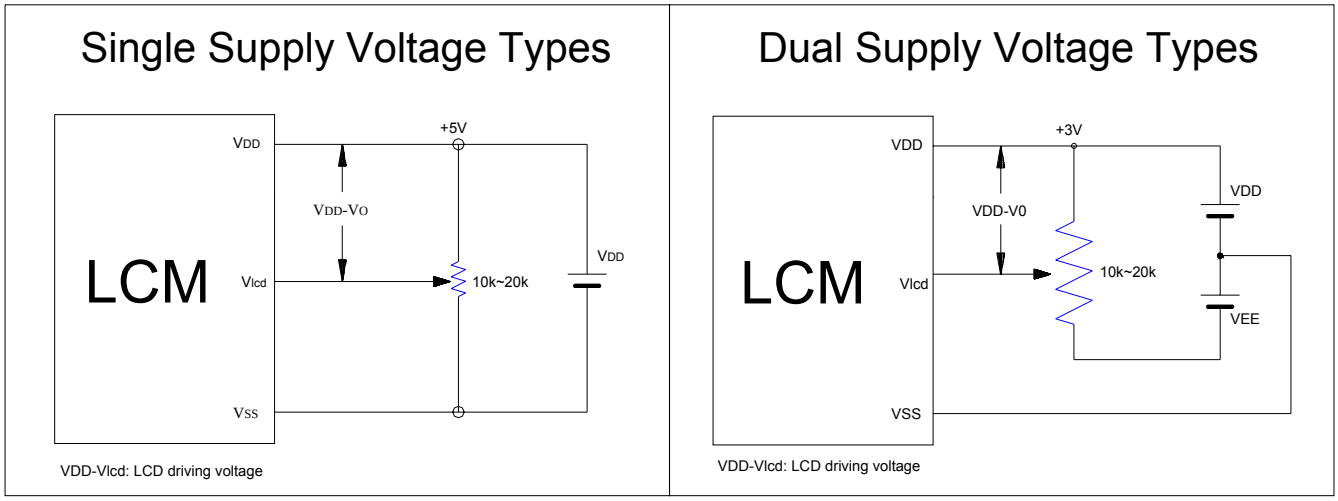
Detects a rising or falling edge of an RES input and initializes the MPU during power-on. • Initialization status

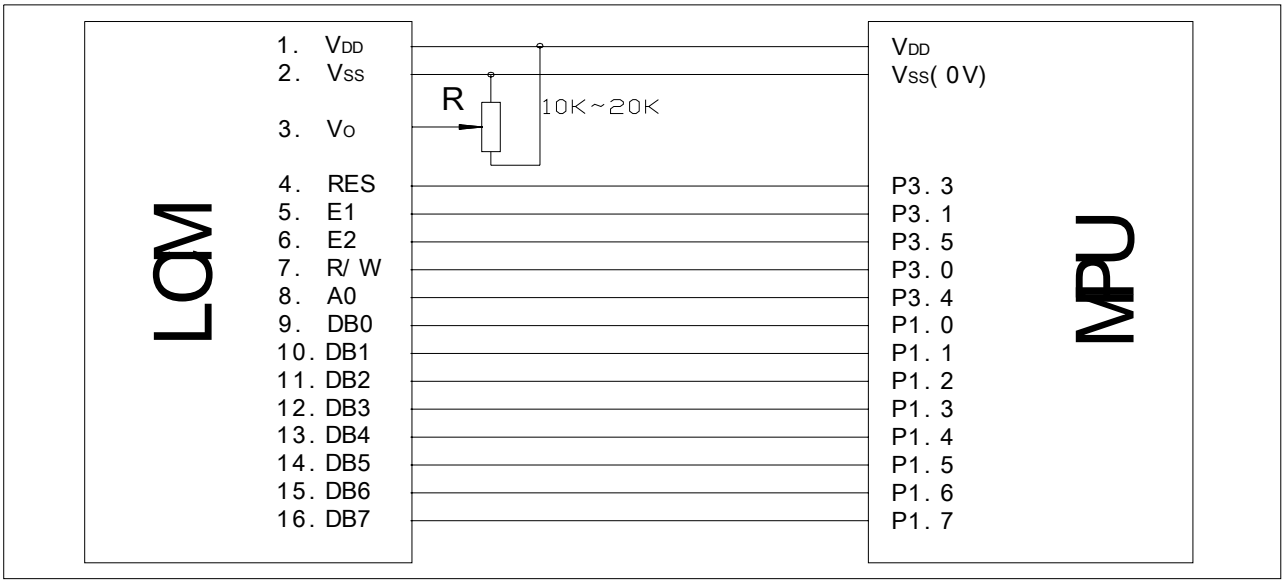
1. Display is off.
2. Display start line register is set to line 1.

3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 3.
6. 1/32 duty or is selected.
7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at RES pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the RES input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered. As shown for the MPU interface (reference example), the RES pin must be connected to the Reset pin and reset at the same time as the MPU initialization. If the MPU is not initialized by the use of RES pin during power-on, an unrecoverable MPU failure may occur. When the Reset command is issued, initialization

c) Example Power Supply





```
          E1        EQU       P3.5
          E2        EQU       P3.1
          RW        EQU       P3.0
          A0        EQU       P3.4
          RES       EQU       P3.3
          DATA1     EQU       40H
          DATA2     EQU       41H

          ORG              0H
          AJMP             START

           ORG           0100H
START:    CLR              RES
          ACALL            DEL1
          SETB             RES
MOV       A,#0AEH             ;Display off
LCALL      OUTI
MOV       A,#0E2H            ;RESET
LCALL      OUTI
MOV       A,#0A9H             ;Duty 1/32
LCALL      OUTI
MOV       A,#0AFH             ;Display on
LCALL      OUTI
MOV       A,#00H            ;Display Column Address
LCALL      OUTI
MOV       A,#0B8H             ;Display page Address
LCALL      OUTI

MOV       DATA1,#55H
MOV       DATA2,#55H
ACALL      LL
MOV       DATA1,#0FFH
MOV       DATA2,#00H
ACALL      LL
MOV       DATA1,#55H
MOV       DATA2,#0AAH
ACALL      LL
JMP START


LL:       MOV       R1,#30
          MOV       R2,#0B8H
LLL:      MOV       A,R2
          ACALL      OUTI
          MOV       A,#00H
          ACALL      OUTI
          MOV       A,#0C0H
          ACALL      OUTI
LL1:      MOV       A,DATA1
          ACALL      OUTL
          MOV       A,DATA2
```

```
        ACALL    OUTL
        DJNZ     R1,LL1
        MOV      A,DATA1
        ACALL    OUTL

        MOV      R1,#30
        MOV      A,R2
        ACALL    OUTI
        MOV      A,#00H
        ACALL    OUTI
RR1:    MOV      A,DATA2
        ACALL    OUTR
        MOV      A,DATA1
        ACALL    OUTR
        DJNZ     R1,RR1
        MOV      A,DATA2
        ACALL    OUTR
        MOV      R1,#30
        INC R2
        CJNE     R2,#0BCH,LLL
        ACALL    DELAY
        RET
OUTI:   CLR      A0
        CLR      RW
        SETB     E2
       SETB      E1
        NOP
        MOV      P1,A
        NOP
        NOP
        CLR      E2
        CLR      E1
        ACALL      DEL1
        RET

OUTL:   SETB     A0
        CLR      RW
        SETB     E2
        MOV      P1,A
        CLR      E2
        MOV      R5,#0FFH
        DJNZ     R5,$
        RET

OUTR:   SETB     A0
        CLR      RW
        SETB     E1
        MOV      P1,A
        CLR      E1
        MOV      R5,#0FFH
        DJNZ     R5,$
```

```
        RET

DEL1:   MOV     r6,#0f4h
        MOV     R5,#02EH
DEL:    DJNZ    R5,$
        DJNZ    r6,DEL
        RET

DELAY:  MOV     R4,#010H
KEY2:   ACALL   DEL1
        DJNZ    R4,KEY2
        RET
        END
```